ABSTRACT OF THE DISCLOSURE

The contact resistance of each switch is reduced, and the on-resistances of all of the switches are set to be uniform, while the area required for arrangement of bit line selection switches is not increased.

The switches are connected to one-side ends of the bit lines provided at the odd-numbered positions, and are connected to the other-side ends of the bit lines provided at the even-numbered positions. A pair of odd-numbered or even-numbered bit lines are connected to the terminals of each sense amplifier, respectively. The memory cells are arranged at predetermined intersection points of the word lies and the bit lines, the number of the predetermined intersection points being equal to half of all the intersection points thereof, in such a manner that when one word line is selected, the memory cells connected to the selected word-line can be electrically connected in such a manner that one memory cell is electrically connected to each terminal of the unit circuits.